Saad Khan

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EDUCATION

Ghulam Ishaq Khan Institute of Engineering Sciences and Technology (GIKI)   Topi, Pakistan
Bachelor of Science in Computer Engineering   Sep 2020 – Jun 2024

- **Academic High Distinction** in 7th and 8th semesters (SGPA: 3.81 and 3.79).

PROFESSIONAL EXPERIENCE

DreamBig Semiconductors   Islamabad, Pakistan
ASIC Verification Engineer   Dec 2024 – Present

- **Team Lead – C3PC Project:** Led a **4-member DV team** for block and chip level UVM verification, coverage closure and regression sign-off with *daily sync-ups* and *weekly global reviews*; managed task assignment, sprint planning and kick-off for an 8-engineer development effort; defined **test requirements** from design specs.

- **Architect and Owner – DV Env. and Scoreboard:** Built the full UVM-based DV environment for the Mercury C3PC complex; Architected a SystemVerilog scoreboard handling **multi-million packet events** across **64 isolation domains**, tracking **8,192 destination IDs** and **TID-based requester/responder matching**.

- **Protocol Agents, Regression and Nightly Runs:** Developed **APB**, **AXI4** and **AXI-Stream** agents with READY VALID and VALID READY handshakes; modeled complex transactions across all interfaces; reduced local regression runtime from **30 min to 5 min** and CI runtime from **40 min to 4 min**; implemented nightly suites to rerun passing tests with instant failure alerts.

- **Bug Hunting and Tracking:** Filed **85+ design bugs** and tracked them to closure; collaborated with RTL to validate fixes and reduce escape rate.

NUST Chip Design Center (NCDC)   Islamabad, Pakistan
RTL Design Engineer   Jun 2024 – Dec 2024

- **Architected RTL** (SystemVerilog) and **FPGA prototyping (Vivado/Quartus)** of synthesizable modules from scratch on **ARTIX-7 FPGA**, including:

  - **UART** with **full-duplex FIFOs**, handshake logic (READY/VALID), and **baud-rate generators**.

  - **Custom/pipelined RISC-V cores** featuring **hazard-detection units, forwarding units, and an integrated branch predictor**. Implemented instruction fetch, decode, execute, memory and writeback stages with precise timing constraints.

  - **Arithmetic IP** such as **carry-lookahead, CSA and CSK**, optimized for minimal propagation delay and balanced **fan-out**.

- **Led** cross-functional design teams for UART, RISC-V, branch-predictor and custom-adder projects; **trained** cohorts on RTL coding best practices, FPGA prototyping workflows, clock-domain crossing strategies, and UVM-based verification, supporting partnerships with AQL and other industry collaborators.

Chip – DV, GIK   Topi-GIKI, Pakistan
Research Assistant   Jun 2023 – Jun 2024

- **Developed and FPGA Prototyped custom RISC-V cores (single-cycle and 5-stage pipeline)** with hazard-detection, **forwarding logic, and branch handling**; **delivered** technical seminars on RISC-V and ASIC design at GIKI.

- **Spearheaded** two first-ever-University **tapeouts via OpenLane (UART transceiver and 24-hour RTC)**, managing **RTL-to-GDSII flow, LVS/DRC sign-off, and ASIC validation**; **implemented** FPGA prototypes of high-speed multipliers (Booth/Wallace-tree) and UART, with UVM/SystemVerilog testbenches.

Musketeers Tech   Lahore, Pakistan
Artificial Intelligence Intern   Jun 2023 – Sept 2023

- **Developed** end-to-end AI solutions: fine-tuned Transformer-based Urdu TTS (Google B2), implemented a ResNet-34 classifier (99% accuracy), **built** a multilingual chatbot (Bi-LSTM/ANN + OpenAI LLM).

TAPEOUTS

- **8-bit UART Transceiver: Led** design and verification of a full-duplex UART with 8-bit data frames and oversampling. **Implemented** in SystemVerilog, verified via UVM testbenches and FPGA Prototyping, and submitted through **Efabless TinyTapeout 6** shuttle targeting the **Sky130 process node** —marking **GIKIs first fabricated chip** [LINK].

- **24-Hour Digital Clock: Directed** RTL-to-GDSII flow for a reset-capable, 24-hour time-format clock, **managing** timing-closure and LVS/DRC sign-off. **Fabricated via TinyTapeout 6 on the Sky130 process node**, achieving the universitys inaugural successful tapeout. [LINK]

SKILLS

Hardware and Verification SystemVerilog, UVM/UVM_REG, SVAs, AXI4, APB, constrained-random testbenches, Cadence, Synopsys

Scoreboarding and Automation Multithreaded SV scoreboard design, credit-starvation and flow-control checks, Jenkins/Tcl pipelines, Confluence documentation

FPGA and RTL Design Vivado, Quartus, Efabless TinyTapeout, RISC-V cores, custom ALUs, hazard detection, timing closure

CI/CD and Scripting C/C++, Python, Bash, Git/GitHub Actions, Docker, Makefiles

AI/ML Acceleration PyTorch, TensorFlow, HuggingFace Transformers

Collaboration and Leadership Sprint planning, daily/weekly syncs, cross-team coordination, recruitment and career-fair outreach

COURSES AND CERTIFICATIONS

- Essential System Verilog for UVM (Cadence)

- System Verilog Accelerated Verification with UVM V1.2.6 (Cadence)

- Application Specific Integrated Circuits, ASIC. (GIKI)

- Unsupervised Learning, Recommenders, Reinforcement Learning (Coursera)

FINAL YEAR PROJECT

INTELLERA: A Hardware Based Accelerated Matrix MAC Processor [LINK]

- **Designed** a custom 5-stage pipelined RISC-V processor (Artix-7, Vivado, Verilog) with full hazard resolution, integrated branch predictor, and support for 18 RV32I base instructions plus **11 custom MATRIX-MAC** instructions using a dedicated **MAC decoder** and **systolic-array-based unit** for 2D operations.

- **Built** a **UART-based loader** (also taped out) to receive instructions byte-by-byte, pack them into 32-bit format, and store them in instruction memory; **enabled** dynamic program loading **without bitstream regeneration** via a custom **Python script**.

ACADEMIC / PROFESSIONAL PROJECTS

- **Parametrized Skid Buffer IP:** Architected a fully-parameterized SystemVerilog skid buffer—configurable depth and width, READY→VALID handshakes, back-pressure support, EMPTY/FULL flags, and built-in SV assertions for failure detection; reusable across AXI, APB, custom interfaces.

- **Single-Cycle RISC-V Processor on FPGA: Designed** a complete single-cycle RISC-V RV32I processor on FPGA using Verilog, with **control unit, ALU, instruction/data memories, decoder, and fully functional register file**, **verified** on **Nexys4** board. [LINK]

- **5-Stage Pipelined RISC-V Processor: Developed** a **fully pipelined 5-stage RISC-V** processor (IF, ID, EX, MEM, WB) with **hazard detection, stall control, branch prediction, and forwarding logic**, **written** in Verilog and **synthesized** on FPGA. [LINK]

- **8-bit UART Transceiver with Baud Rate Selection: Engineered** an 8-bit UART transceiver supporting multiple baud rates via configurable baud rate generator; **tested** and **deployed** on Artix-7 FPGA, supporting TX/RX buffering and oversampling. [LINK]

- **UVM-Based UART Verification Environment: Developed** a complete UVM testbench for verifying the UART transceiver; **implemented** agents, sequencers, monitors, drivers, and a functional scoreboard with support for randomized packet testing and protocol checking.

- **VGA-Based Pong Game on Nexys4 FPGA: Implemented** a real-time Pong game using Verilog and VGA controller logic on Nexys4 FPGA, demonstrating digital design, state machines, and pixel timing control.

- **18-DOF Hexapod Robot: Built** a 3D-printed 18-DOF hexapod using Raspberry Pi, **designed** inverse kinematics, **developed** multithreaded Python control software, a custom GUI, and a TCP server for real-time remote control.

LEADERSHIP EXPERIENCE

Coordinator Operations – GIKI Science Society   May 2023 – May 2024
Pioneered the successful back-to-back All Paks (ISYS, APSF) within one fiscal year, **achieving** unprecedented participant registration growth from 200 to 350 and 120 to 200 respectively, **surpassing** previous records by 75% and 66%.

Testing and Design Head – GIKI Team Invictus   Nov 2021 – May 2023
Testing aircraft components and modules to ensure performance and safety. **Directed** design team, **fabricated** multiple compact streamline UAVs with speeds over 100 km/h.